We claim:

1. A memory comprising:

memory transistors arranged in a group;

a drive circuit coupled to a memory transistor of the group so that information can be written to and read from the memory transistor; and

a selection transistor coupled with the group of memory transistors so that the group of memory transistors can be jointly selected.

2. The memory according to claim 1, wherein the group of memory transistors has 16 to 32 memory transistors.

3. The memory according to claim 1, wherein the group of memory transistors is arranged in at least one of a row and a column.

4. The memory according to claim 2, wherein the group of memory transistors is arranged in at least one of a row and a column.

5. A method for operating a memory, comprising the steps of:

providing memory transistors arranged in a group of at least one of a row and a column;

providing a drive circuit coupled to a memory transistor of the group so that information can be written to and read from the memory transistor;

providing a selection transistor coupled with the group of memory transistors so that the group of memory transistors can be jointly selected;

opening the selection transistor while gate terminals of the memory transistors of the group of memory transistors are at low potential;

measuring a first current flowing through each row or column to be read;

storing the measured first current;

supplying a read potential to gate terminals of the row or column to be read;

measuring a resulting second current flowing through the row or column to be read; and

comparing the second current with the stored first current.

6. A memory comprising:

means for providing memory transistors arranged in a group of at least one of a row and a column;

means for providing a drive circuit coupled to a memory transistor of the group so that information can be written to and read from the memory transistor;

means for providing a selection transistor coupled with the group of memory transistors so that the group of memory transistors can be jointly selected;

means for opening the selection transistor while gate terminals of the memory transistors of the group of memory transistors are at low potential;

means for measuring a first current flowing through each row or column to be read;

means for storing the measured first current;

means for supplying a read potential to gate terminals of the row or column to be read;

means for measuring a resulting second current flowing through the row or column to be read; and

means for comparing the second current with the stored first current.

7. A method for operating a memory having memory transistors arranged in a group, a drive circuit coupled to a memory transistor of the group so that information can be written to and read from the memory transistor, and a selection transistor coupled with the group of memory transistors so that the group of memory transistors can be jointly selected, the method comprising the steps of:

opening the selection transistor while gate terminals of the memory transistors of the group of memory transistors are at low potential;

measuring a first current flowing through each row or column to be read;

storing the measured first current;

supplying a read potential to gate terminals of the row or column to be read;

measuring a resulting second current flowing through the row or column to be read; and

comparing the second current with the stored first current.